Hall Ticket Number:

Code No. : 13607

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (IT: CBCS) III-Semester Main Examinations, December-2017

Digital Electronics & Logic Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Derive canonical SOP expression for the Boolean function $f\ (x1, x2, x3) = \sum(2,3,4,6,7)$.
2. Simplify the following expression to minimum number of literals.
   $F = xyz + x'y + xyz'$.
3. Design a 1 × 4 Demultiplexer.
4. Distinguish between PLA and PAL.
5. Show the construction of SR latch circuit using NAND gate and also give its truth table.
6. Construct the excitation table for T flipflop.
7. Illustrate the general structure of sequential circuit
8. Discuss State minimization and state assignment?
9. Illustrate the concept of Clock Skew?
10. Discuss about ASM charts.

Part-B (5 × 10 = 50 Marks)
(All bits carry equal marks)

11. a) Check the validity of the following equation using truth table.
    $\overline{x_1}\ \overline{x_3} + x_2 x_3 + x_1 \overline{x_2} = \overline{x_1} x_2 + x_1 x_3 + \overline{x_3}\ \overline{x_2}$
    b) Simplify the Boolean function using Karnaugh Map.
    $F(w, x, y, z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$.

12. a) Implement the following functions using schematic of PAL.
    $f_1 = x_1 x_2 + x_1 \overline{x_3} + \overline{x_1}\ \overline{x_2} x_3$ & $f_2 = x_1 x_2 + x_1 x_3 + \overline{x_1}\ \overline{x_2} x_3$
    b) Design 2-to-1 multiplexer and support with truth table and write the VHDL code for the same.

13. a) Explain JK-Flip Flop and master slave JK Flip Flop with the help of diagrams.
    b) Design BCD ripple counter and explain its operation with timing diagrams.

14. a) Illustrate state diagram and state table for Modulo-8 Counter.
    b) Design Mealy type sequence detector to detect the 101 sequence from the input sequence.

15. a) Explain about Races and cycles in asynchronous sequential circuits.
    b) Outline static and dynamic hazard with proper example.

16. a) Implement the function $f = (x_2 + x_1\ \overline{x_3})$ using NAND gates.
    b) Draw FPGA configuration and explain how a Boolean function can be implemented using 2 i/p and 3 i/p LUTs.

17. Answer any ***two*** of the following:
    a) Illustrate the concept of shift registers.
    b) Implement a 3 bit synchronous up counter in VHDL.
    c) Explain with numerical example how 6 bit multiplication performed using shift and add method.